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[54] **GTO THYRISTOR CAPABLE OF PREVENTING PARASITIC THYRISTORS FROM BEING GENERATED**

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[58] **Field of Search** 257/119, 122, 124, 128, 257/132, 133, 135, 138, 147, 150, 152, 153, 154, 163, 167

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,760,431	7/1988	Nakagawa et al.	257/138
4,967,255	10/1990	Bauer et al.	257/153
5,105,244	4/1992	Bauer	257/138
5,144,400	9/1992	Bauer	257/138

FOREIGN PATENT DOCUMENTS

61-58264	3/1986	Japan	257/138

OTHER PUBLICATIONS

Baliga, Proceedings of 1990 International Symposium on Power Semiconductor Devices & ICs, pp. 117-121. "The MOS-Gated Emitter Switched Thyristor".

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[57] **ABSTRACT**

A GTO thyristor includes a p-type emitter layer, an n-type base layer, a p-type base layer and an n-type emitter layer. An additional n-type layer is formed on the p-type base layer next to the n-type emitter layer An additional p^+-type layer is formed on the additional n-type layer and stretches to the n-type emitter layer. An anode electrode and a cathode electrode are disposed respectively on the n-type emitter layer and the p-type base layer. The n-type emitter layer and the additional p^+-type layer are connected with each other by a floating electrode. A first gate electrode is disposed on the additional p^+-type layer, additional n-type layer and p-type base layer with an insulating film interposed therebetween so as to form a first FET. A second gate electrode is disposed on the n-type base layer, p-type base layer and n-type emitter layer with an insulating film interposed therebetween so as to form a second FET. A thyristor having such a configuration can effectively prevent a latched-up condition caused by parasitic transistors or thyristors to ensure turn off operations of the host thyristor.

16 Claims, 18 Drawing Sheets